

Consumer and
Corporate Affairs CanadaConsommation
et Corporations Canada

1 255 406

(11) (A) No.

(45) ISSUED 890606

(52) CLASS 375-53

(51) INT. CL. ⁴ G09G 3/20(19) (CA) **CANADIAN PATENT** (12)(54) Electronic Circuit Formed from Thin Film Transistors
tor Controlling a Matrix Device(72) Morin, François;
Sargent, Jacques;
Delaplace, Stéphan,
France(73) Granted to l'Etat Français représenté par le
Ministre des PTT (Centre National d'Etudes des
Télécommunications), France

(21) APPLICATION No. 496,472

(22) FILED 851128

(30) PRIORITY DATE (FR) France (84 18110) 841128

No. OF CLAIMS 2

Canada

DISTRIBUTED BY THE PATENT OFFICE, OTTAWA.

CDA-27-111-451

1255406

-1-

ELECTRONIC CIRCUIT FORMED FROM THIN FILM TRANSISTORSFOR CONTROLLING A MATRIX DEVICE

The present invention relates to an electronic circuit formed from thin film transistors (TFT) used for controlling a matrix device.

More specifically, the invention relates to an electronic circuit of the shift register type used for sequentially controlling the rows or columns of a matrix device and more particularly the rows or columns of a liquid crystal display (flat-faced screen with active matrix, screen for instrument panel, etc), photosensitive video "retinas" with thin film transistors, optical sensors or restoration heads for telecopying systems having rows of photodiodes, sensors, etc.

In an active matrix-type screen, an electronic memory formed from memory points distributed over the entire surface of the screen, stores the video signal for the duration of the image. An electrooptical transducer, particularly a liquid crystal, is in contact with each memory point and is excited for the duration of the image. Each memory point is located at the intersection of a connecting row and column and is constituted by a thin film transistor produced on an insulating support and a capacitor, whose coatings are formed in the case where the transducer is a liquid crystal by the electrodes of the liquid crystal cell, the insulating support forming one of the two walls of said cell.

The electronic circuits of the shift register type considered for controlling such a active matrix have been studied in TFT technology, but as they are so complex it has not proved possible to produce them on a large scale.

Thus, it is very difficult to produce a shift register

B 8304.C LC

*
*

1255406

-2-

with thin film transistors, particularly when it must have a very large number of stages (300 to 500 and even more, as a function of the number of rows or columns of the flat-faced screen) and if there is any defect the 5 screen will not function.

Each stage of the shift register generally has two elementary inverters and a capacitor for storing the video information. Moreover, each inverter is formed from at least two thin film transistors arranged in 10 cascade.

As the thin film transistors of the active matrix are generally produced with amorphous silicon, they have a low transconductance and a high input capacitance, so that relatively low operating limit frequency for the 15 inverters is obtained and which is usually below the scanning frequency of the rose of a very complex flat-faced screen (300 to 500 rows).

Moreover, the operation of such a shift register is highly dependent on the homogeneity of the 20 characteristics of the thin film transistors, so that the efficiency is not very high.

It has also been considered to produce shift registers of the charged transfer type, known as bucket brigade devices (BBD) or charge-coupled devices (CCD), which 25 require fewer thin film transistors, but whereof the fault density in the amorphous silicon has led to an inefficiency of the transfer of charges.

It is for this reason that in existing active matrix flat screens, the peripheral control circuits of these 30 screens are not integrated therewith, the control of the screens being ensured by standard integrated circuits located outside them. Unfortunately, in such a system, it is necessary to arrange a large number of boxes on a

B 8304.C LC

1255406

-3-

printed circuit connected to the flat-faced screen, which causes problems of complex, difficult connections, or alternatively the corresponding integrated circuits or chips must be placed on the glass support, so that a 5 large number of welds have to be made.

In certain externally controlled flat-faced screens, the cost thereof is high due to the cost of the control circuits and the number of connections to be produced between the flat-faced screens and the corresponding 10 circuits, or the number of welds to be made on the glass support. It is generally accepted that the peripheral integrated circuits, i.e. all the row and column control circuits of the flat-faced screen amount to half and even more of the total costs for said screen.

- 15 The present invention is directed at an electronic circuit formed from thin film transistors used for controlling matrix devices and particularly active matrix flat-faced screens making it possible to obviate the aforementioned disadvantages. In particular, it 20 makes it possible to simplify the connection of the peripheral integrated circuits with the active matrix, whilst minimising the cost of said circuits and consequently the total price of the flat-faced screens by reducing the number of such peripheral circuits.
- 25 Thus, the invention relates to an electronic circuit for controlling the rows or columns of a matrix device and using on the one hand standard integrated circuits outside the device for ensuring the shift register function and on the other hand thin film transistors for 30 ensuring the multiplexing function.

More specifically the present invention relates to an electronic control circuit $N \times n$ outputs used for controlling $N \times n$ rows or columns of a matrix device and more particularly a matrix display, wherein it comprises

B 8304.C LC

1255406

-4-

a multiplexing circuit, formed from N groups of n successive thin film transistors, a first shift register with N outputs and a second shift register n outputs, the gates of the n transistors of the same group being 5 connected to the same output of the first register, whereby to each group corresponds a different output of said first register, the source of each transistor being connected to a different row or column, the drain of the ith transistor of each group being connected to the ith 10 output of the second register, i being an integer such that $1 \leq i \leq n$.

The term matrix device is understood to mean a device having only a single row or column of components.

These electronic control circuits only have two external 15 integrated circuits, which are the two shift registers making it possible to supply via the multiplexing circuit, NxN rows or columns of a matrix device and more particularly an active matrix flat-faced screen. Thus, it is possible to reduce the number of connections to be 20 made between the external circuits and the flat-faced screen, as well as to reduce the cost of such screens.

When the electronic circuit according to the invention makes it possible to control the NxN rows or columns of a matrix device having thin film transistors formed on 25 the same insulating support, the thin film transistors of the multiplexing circuit of the control circuit according to the invention can be advantageously realised on said support and simultaneously with the transistors of the matrix device.

30 Other features and advantages of the invention can be gathered from the following non-limitative description. For reasons of clarity, this description refers to the control of the rows of an active matrix flat-faced screen, but obviously the invention has a much more

B 8304.C LC

1255406

-5-

general application, as stated hereinbefore. The description refers to the attached drawings, wherein show :

Fig 1. Diagrammatically an electronic circuit according 5 to the invention for controlling the rows of an active matrix flat screen.

Fig 2. The different input and output signals of the control circuit of fig 1.

Fig 1 shows an electronic control circuit according to 10 the invention making it possible to control the $N \times n$ rows of an active matrix flat-faced screen 2. This active matrix 2 is formed in conventional manner from several conducting columns 4 and $N \times n$ conducting rows L_j , j being an integer between 1 and $N \times n$. At each 15 intersection of a column 4 and a row L_j is located a memory point 8 of the active matrix 2, formed from a thin film transistor 10 and a capacitor 12 connected in series.

This active matrix 2 also comprises $N \times n$ capacitors 14, 20 one of the coatings of each capacitor being connected to earth and the other to one of the conducting rows L_j of the matrix 2.

According to the invention, the control circuit of the $N \times n$ conducting rows L_j of the matrix 2 is constituted 25 on the one hand by a multiplexing circuit 16, formed from N groups G_1, \dots, G_n of thin film transistors, each group G_i having n successive transistors T_1, \dots, T_n and on the other hand a first shift register 18, having N outputs and a second shift register 20 having n outputs.

The multiplexing circuit 16 has one thin film transistor per conducting line L_j , i.e. in all $N \times n$ TFT, e.g for a flat screen with 320 rows, N can be = to 40 and n = to 8.

B 8304.C LC

1255406

-6-

Such a control circuit make it possible to greatly reduce the number of connections to be made between the control circuit and the active matrix, said connections being reduced to $N+n$ connections instead of $N \times n$ connections for the matrix devices according to the prior art.

According to the invention, each conducting row L_j of the active matrix 2 is supplied by the source of a single TFT, e.g. the source of the first transistor T_1 of group G_1 is connected to row L_1 , the source of the second transistor T_2 of group G_2 is connected to row L_2 and so on and the source of the final transistor T_N of group G_N is connected to row L_{N-n} .

15 The gates of the N consecutive transistors T_1, \dots, T_n of the same group G_i are connected to the same output P_i of the first shift register 18, a different output P_i of said first register corresponding to each group. In other words, the gates of the transistors T_1, \dots, T_n of the first group G_i of transistors are all connected to output P_i of the first register 18 and the gates of the transistors T_1, \dots, T_n of group G_N of transistors are all connected to output P_N of the first register 18.

25 For the drains of the $N \times n$ thin film transistors, they are supplied in such a way that the drain of the i th transistor T_i of each group G_i is connected to the i th output S_i of the second register 20, i being an integer such that $1 \leq i \leq n$. In other words, the first 30 transistors T_1 of each group of transistors G_1, \dots, G_n are all connected to the first output S_1 of the second shift register 20, the second transistor T_2 of the groups of transistors G_1, \dots, G_n are all connected to output S_2 of the second register 20 and 35 so on and the final transistors T_n of groups G_1, \dots, G_n

B 8304.C LC

1255406

-7-

G_1, \dots, G_n of transistors are all connected to the final output S of the second register 20.

Fig 2 shows the different input and output signals of the control circuit of fig 1. Signal $R(n)$ corresponds to the output signal of shift register 20, signal $R(N)$ corresponds to the output signal of shift register 18 and signal L corresponds to the input signal of the first conducting row of matrix 2. Each pulse of duration τ supplied by register 20 corresponds to the access time to a conducting row of the matrix, τ being close to 64 μ s and pulse τ' supplied by register 18 is equal to $n \times \tau$.

A voltage pulse τ supplied by shift register 18 functioning at the scanning frequency of the rows of the flat-faced screen will only be transmitted to a row of said screen in group G_1 made conductive by pulse τ' supplied by shift register 18. When the thin film transistors are non-conductive, the corresponding rows of the flat-faced screen are kept at low level as a result of the row capacitor 14, which remains charged or loaded throughout the duration of an image or picture on the screen.

According to the invention, when the transistors 10 of the active matrix 2 are thin film transistors formed on an insulating support, such as of glass, constituting more particularly one of the two walls of the flat-face screen between which is arranged the liquid crystal, the thin film transistors of the multiplexing circuit 16 can be advantageously produced on said support and simultaneously with the production of the transistors 10 of the active matrix 2 of the screen. However, the two shift registers 18 and 20 will be standard integrated circuits produced independently of the active matrix 2.

One of the processes which can be used for producing the

B 8304.C LC

1255406

-8-

thin film transistors of the multiplexing circuit 16 at the same time as those of the active matrix 2 has been described in French patent publication 2,533,072, filed on september 14. 1982 in the name of the Applicant 5 entitled "Process for the production of electronic circuits based on thin film transistors and capacitors". As is indicated therein, this process also makes it possible to simultaneously produce matrix capacitors such as 12 and 14.

10 In a simplified manner, this production process consists of depositing on an insulating support, such as glass, forming one of the walls of the flat-faced screen, a transparent conductive coating, particularly of tin oxide and indium and then a doped n amorphous silicon 15 coating. These coatings then undergo photogravure with the aid of a first mask, so as to form the sources and drains of the thin film transistors of the multiplexing circuit and the matrix, one of the coatings of the capacitors 12 and 14, the conducting columns 4 of the 20 matrix, as well as the drain bus of the multiplexing circuit 16.

This is followed by the successive deposition of a hydrogenated amorphous silicon coating, an insulating coating, particularly of silicon oxide and a conductive 25 coating e.g. of aluminium. The stack of coatings is then subject to photogravure using a second mask, so as to find the gate of the thin film transistors of multiplexing circuit 16 and matrix 2, as well as the conducting rows L_j of said matrix.

30 The assembly is then passivated with the aid of a deposit of an e.g. silicon oxide coating, after which openings are made in the passivation coating (by photogravure using a third mask) at the ends of the conducting rows of the matrix, on the gates of the thin 35 film transistors of the multiplexing circuit 16 and on

1255406

-9-

the drain bus of said circuit.

This is followed by making a metal deposit, e.g. of aluminium, followed by the photogravure thereof using a fourth mask, so as to form the connections between

5 multiplexing circuit 16 and active matrix 2, between the drain bus and the drains of the thin film transistors of the multiplexing circuit and between the gates of transistors T_1, \dots, T_n of a same group G_i of transistors of multiplexing circuit 16.

10 For further details regarding the production of such electronics circuits based on thin film transistors and capacitors, reference should be made to the aforementioned French patent application.

The application of the electronic circuit according to

15 the invention to the control of the rows of a flat-face screen with active matrix is obviously only an example. In particular, the circuit according to the invention can be used with advantage for controlling the rows of a photosensitive video retina with thin film transistors.

20 Such a retina has in particular been described in French patent publication 2,523,371, filed on March 10, 1982 in the name of the Applicant and entitled "Photoconductive hydrogenated amorphous silicon carbide element and video retina cell using such an element". Moreover, the

25 circuit according to the invention can be used for controlling an array of photodiodes used in telecopying, said photodiodes and the thin film transistors of the multiplexing circuit being produced simultaneously on the same support.

30 In more general terms, the circuit according to the invention can be used for controlling any row of electronic components of the integrated diode or transistor type.

1255406

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. An electronic control circuit having $N \times n$ outputs for controlling $N \times n$ conductive lines of a matrix device, such as a matrix display, comprising: a single multiplexing circuit formed from N groups of n first successive thin film transistors, a first shift register with N outputs, and a second shift register with n outputs, the gates of said first n transistors of the same group being directly connected to the same output of the first register, whereby to each group corresponds a different output of said first register, the source of each first transistor being directly connected to a different conductive line, the drain of the i th first transistor of each group being directly connected to the i th output of said second register, i being an integer such that $1 \leq i \leq n$.
2. An electronic circuit according to claim 1, comprising second thin film transistors, both said first and second transistors being provided on one insulating support.

10

*

496472

-11-

ABSTRACT

Electronic circuit formed from thin film transistors for controlling a matrix device.

This circuit comprising $N \times n$ outputs for controlling $N \times n$ rows of a matrix device is characterized in that,

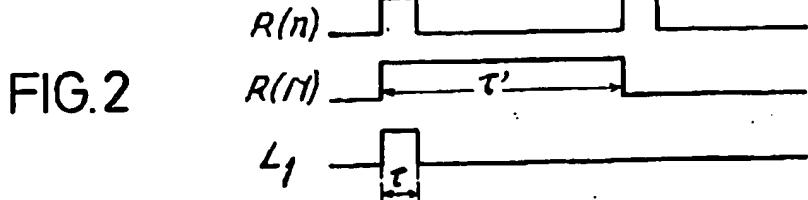
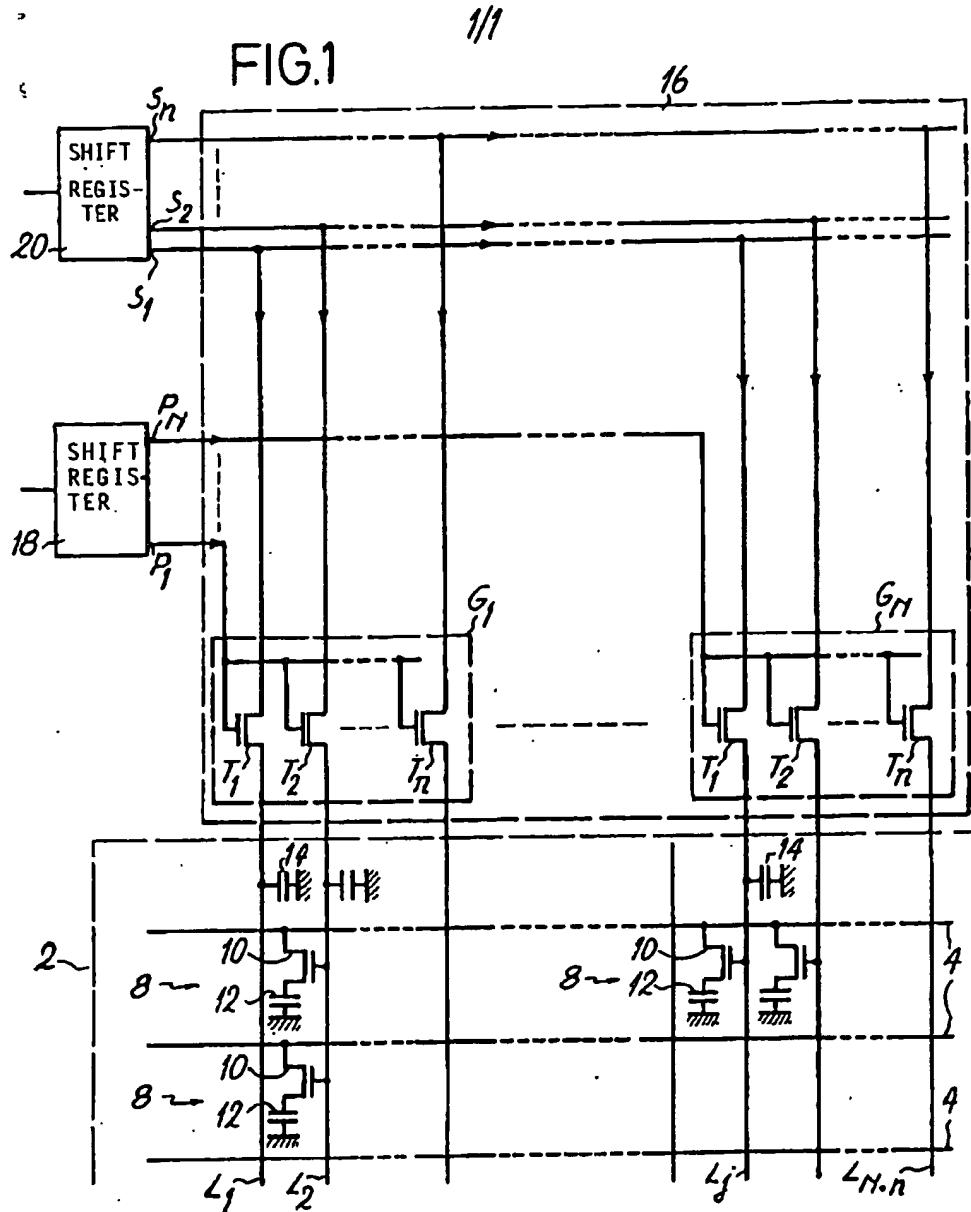
5 it comprises a multiplexing circuit, formed from N groups of n successive thin film transistors, a first shift register with N outputs and a second shift register n outputs, the gates of the n transistors of the same group being connected to the same output of the

10 first register, whereby to each group corresponds a different output of said first register, the source of each transistor being connected to a different row or column, the drain of the i th transistor of each group being connected to the i th output of the second

15 register, i being an integer such that $1 \leq i \leq n$.

B 8304.C LC

1255406



B 8304C

Landau, Sage, Dubuc & Martineau, Waller